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Logic Design Lab Viva Questions

Digital Logic Design VIVA Questions :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock

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400+ TOP Digital Logic Design VIVA Questions and Answers

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16 TOP Digital Logic Design VIVA Questions and Answers ...

250+ Digital Logic Design Interview Questions and Answers, Question1: Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Question2: What is skew, what are problems

associated with it and how to minimize it? Question3: What is slack? Question4: What is glitch? What causes it (explain with waveform)?

TOP 250+ Digital Logic Design Interview Questions and ...

Logic Design Laboratory Manual 3 _____ VIVA QUESTIONS: 1. Why NAND & NOR gates are called universal gates? 2. Realize the EX – OR gates using minimum number of NAND gates. 3. Give the truth table for EX-NOR and realize using NAND gates? 4. What are the logic low and High levels of TTL IC's and CMOS IC's? 5. Compare TTL logic family with ...

LOGIC DESIGN LABORATORY MANUAL - ElectricVLab

1 CCN2272 Logic Design – Lab01 discussion worksheet Discussion questions for Lab01 1a. Logic gates 1. Consider setup A (the switch is above the 10k Ω resistor). Fill in the table below: Action Input Voltage Output Voltage State of LED Leave the

switch open (off) Press to close the switch (on) 2. Consider setup B (the switch is below the 10k Ω resistor). Fill in the table below: Action ...

Lab01_Discussion_Questions.pdf - CCN2272 Logic Design ...

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For any questions about this text, please email: drexel@uga.edu ... Introduction to Digital Logic with Laboratory Exercises 6 A

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Introduction to Digital Logic with Laboratory Exercises

For a state machine with 9- 16 states, a binary FSM only requires 4 flip-flops while a one hot FSM requires a flip-flop for each state in the design FPGA vendors frequently recommend using a one hot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a one hot FSM design is typically smaller than most binary encoding styles.

Interview and viva questions and answers on Digital ...

ANALOG ELECTRONICS VIVA & INTERVIEW QUESTIONS PROF. HITESH DHOLAKIYA Ans Slew rate is the maximum rate of change of output voltage per unit of time. Q-12 What do you

mean by gain band width product of an op-amp? Ans The gain bandwidth of an op-amp is the “bandwidth when the voltage gain is unity”.

Analog Electronics viva & interview questions

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1) Explain how logical gates are controlled by Boolean logic? In Boolean algebra, the true state is denoted by the number one, referred as logic one or logic high. While, the false state is represented by the number zero, called logic zero or logic low.

And in the digital electronic, the logic high is denoted by the presence of a voltage potential.